The NOνA APD Readout Chip

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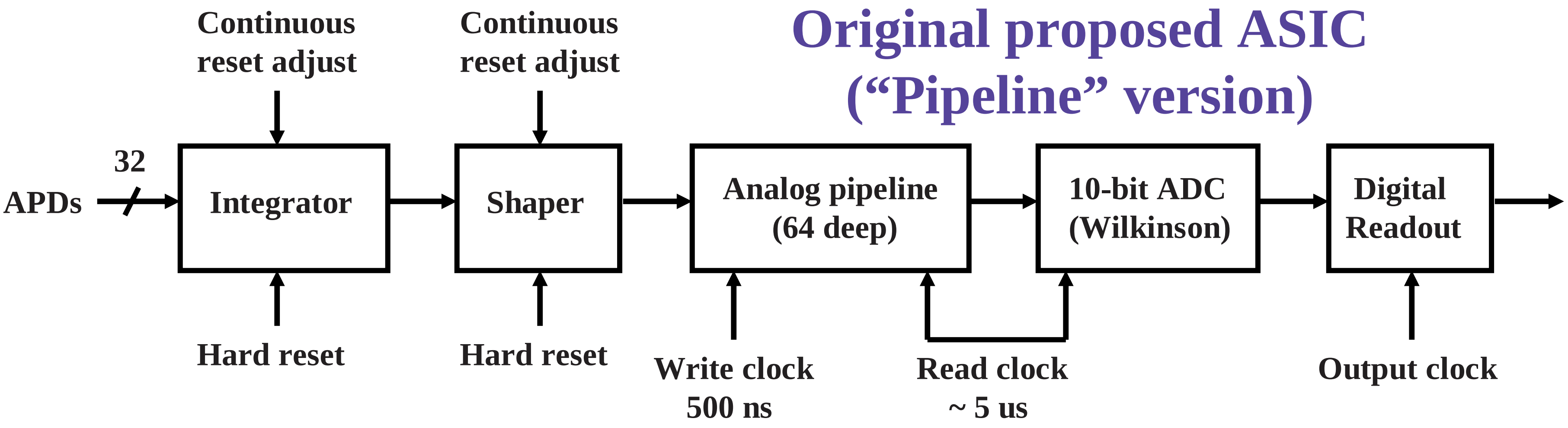
NOνA Detector Readout Requirements

- Record neutrino signal from detector APDs (APD gain ~ 100, C ~ 10pF)
- MIP ~ 25 pe gives 2500e input signal
- Need low noise front end (< 200 e)
- 10 us long beam spill every 2 seconds
- Beam spill arrival known to +/- 10 us
- Integrate APD signals in 500 ns buckets during a 30 us window
- After acquisition, perform Dual Correlated Sampling (DCS) and digitize to extract pulse height and timing
- LSB ~ 100e, max. input = 100Ke: 10-bit dynamic range
- Measurement resolution required = a few percent



Original proposed ASIC
(“Pipeline” version)

Continuous reset adjust

Continuous reset adjust

APDs

32

Integrator

Shaper

Analog pipeline (64 deep)

10-bit ADC (Wilkinson)

Digital Readout

Hard reset

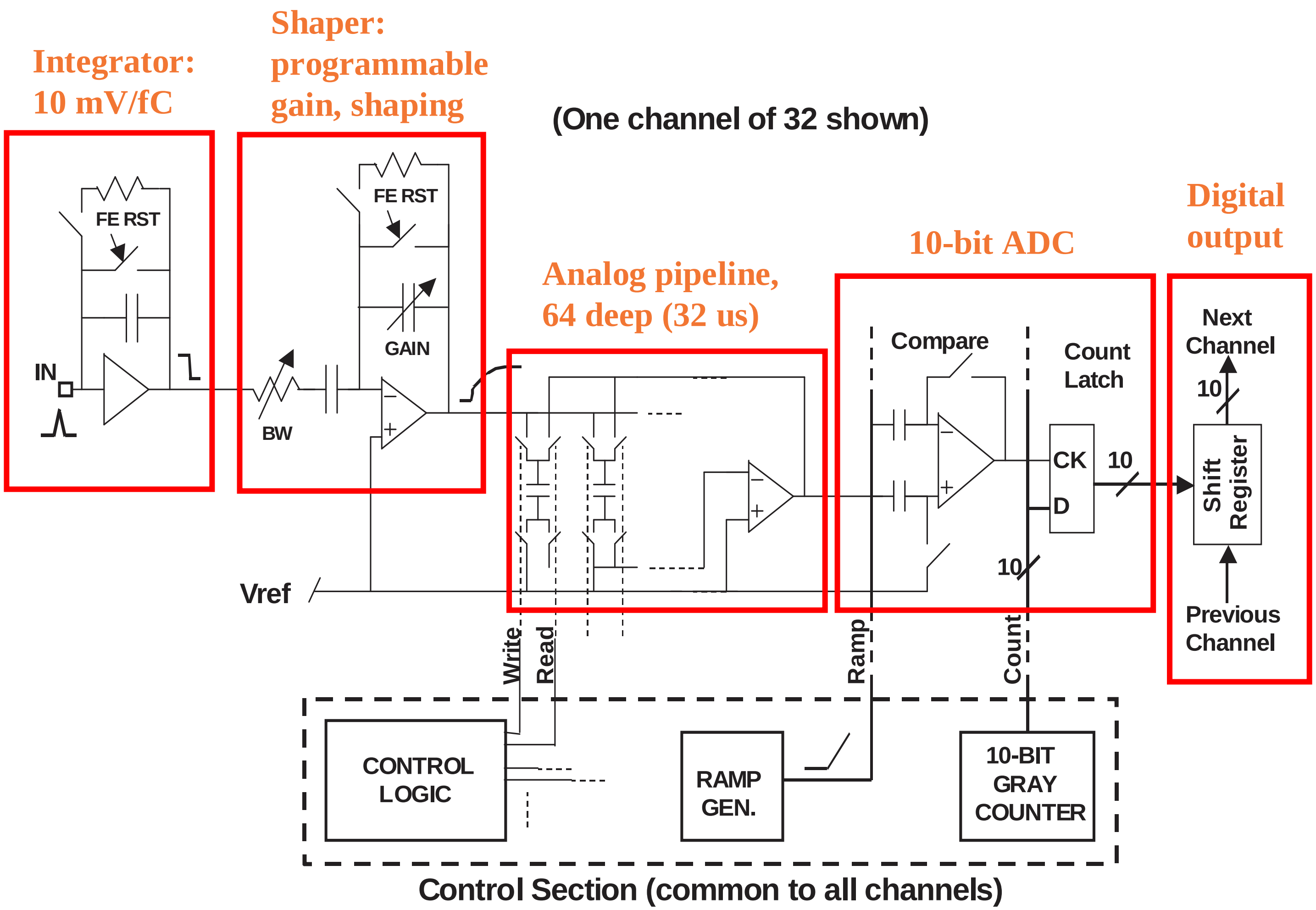
Hard reset

Write clock 500 ns

Read clock ~ 5 us

Output clock

“Pipeline” version design



Integrator: 10 mV/fC

Shaper: programmable gain, shaping

(One channel of 32 shown)

Analog pipeline, 64 deep (32 us)

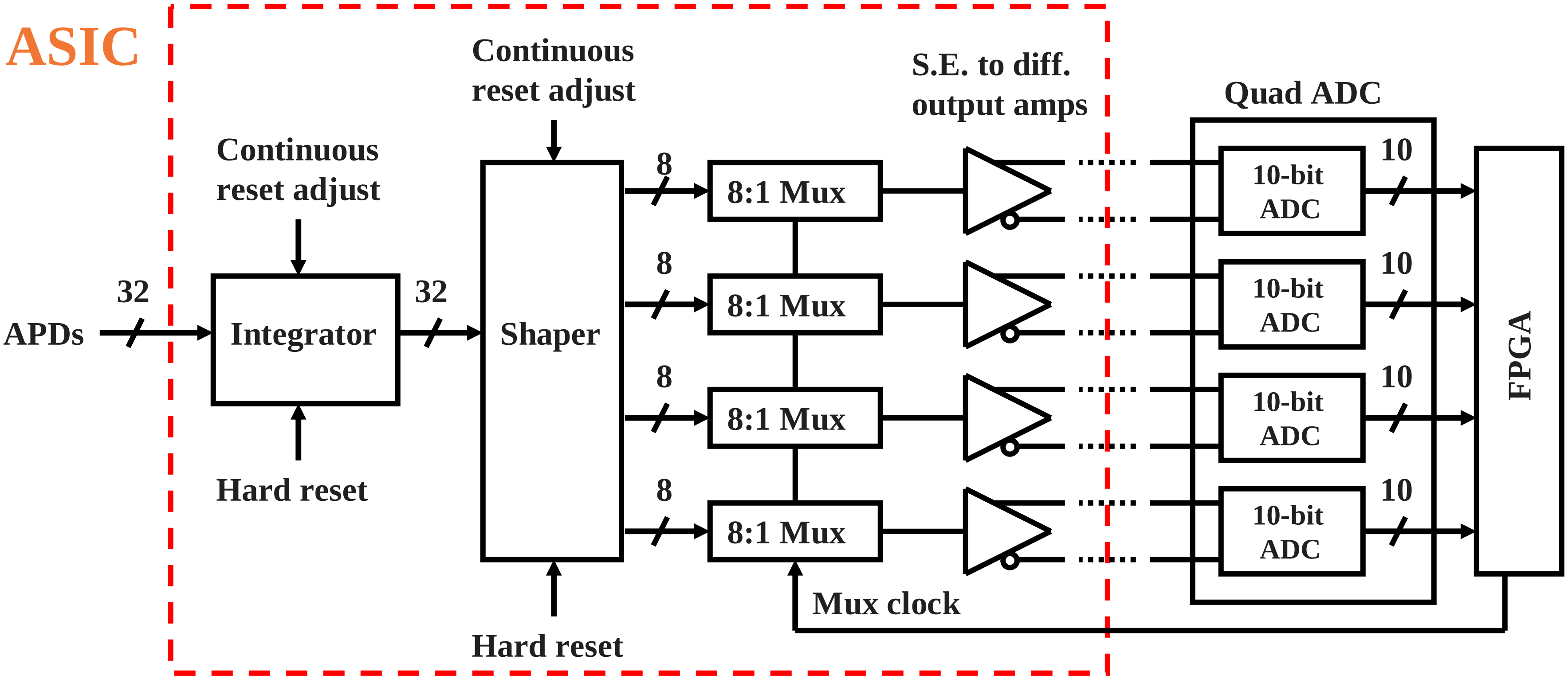
10-bit ADC

Digital output

Control Section (common to all channels)

Alternate ASIC configuration ("Mux" version)

- Would also like to detect supernova neutrino signal (capture 10s of seconds)
- Requires near 100% live time (continuous acquisition and digitization)
- Use four 8:1 analog multiplexers with external ADCs. Multiplex and digitize at 8 X [sample freq.] = 8 X [1/500ns] = 16 MHz. Perform DCS and additional processing digitally in FPGA
- Risk: coupling to low noise front end from continuous digitize/readout



Which approach for **NOνA** ?

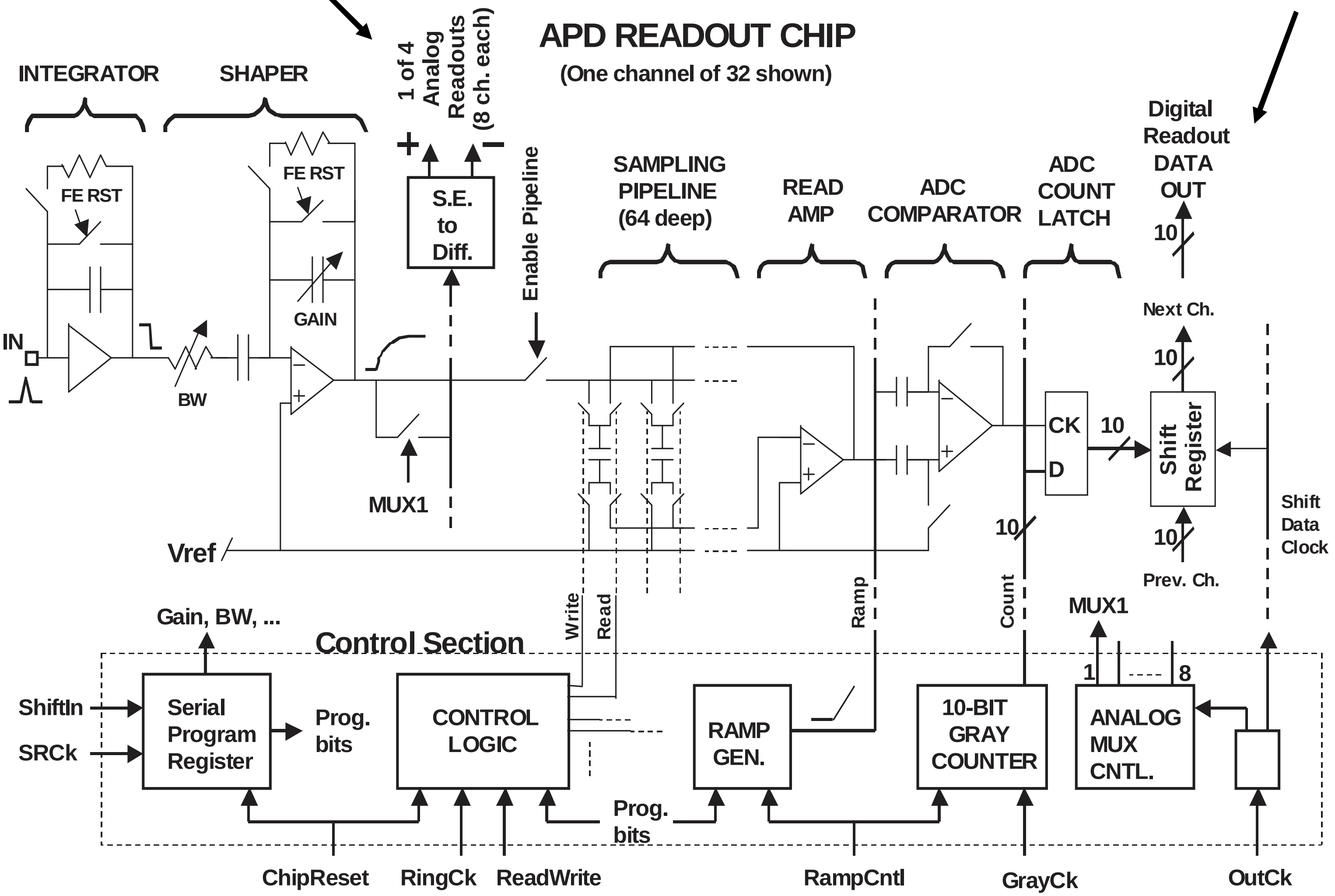
- **Baseline approach:** "Mux" ASIC with external ADCs, allowing 100% live time. Required: ASIC + Quad ADC + FPGA.
- **Backup approach:** "Pipeline" ASIC, allowing separate acquire/digitize cycles if necessary. Required: ASIC + FPGA.

- **Prototype ASIC**: integrate both approaches on one chip, giving maximum flexibility for optimizing the APD readout strategy. Use TSMC 0.25 micron process.

NOνA prototype ASIC

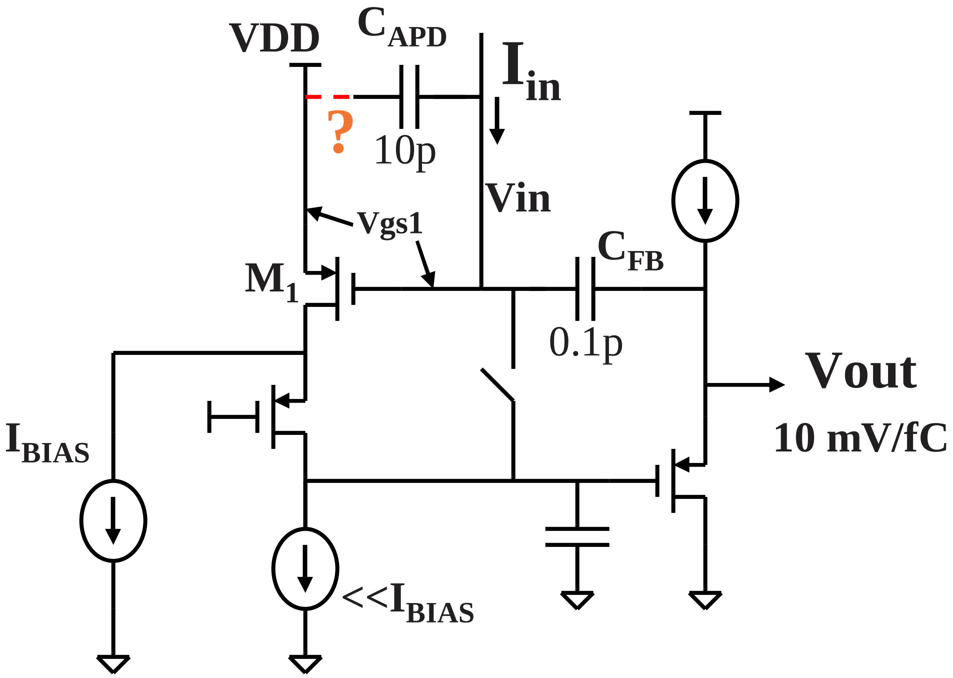
Mux version
analog output

Pipeline version
digital output



Integrator

- 1 LSB ~ 100e: use 10 mV/fC (C_{FB} = 0.1pF), followed by shaper gain (x2-x10)
- 500 ns sample time: M_1 is PMOS to avoid significant 1/f noise contribution.
- M_1 (PMOS) source is referred to VDD, not ground.
- Where to refer APD capacitance for best PSRR?
- If I_{BIAS} is fixed, then Vgs1 is constant, so △Vin = △VDD. If C_{APD} grounded: **△Vout/△VDD** = △Vout/△Vin = C_{APD}/ C_{FB} = **100 (disaster!!)**
- If C_{APD} is referred to VDD:
  - Tight input loop (minimizes pickup)
  - **△Vout/△VDD = 1 (better!!)**



- But what about C_{STRAY} to ground (bond pad, bondwire, etc.)? Ruins PSRR.
- Use M_2 with Vgs = VDD to generate I_{BIAS}.

  Two advantages:

  - 1. For a given I_{BIAS}, **max. Vgs_2** yields **min. gm_2, lowest M_2 noise**.
  - 2. I_{BIAS} changes with VDD. Now △Vin = (△VDD)[1 - (gm_2/gm_1)].

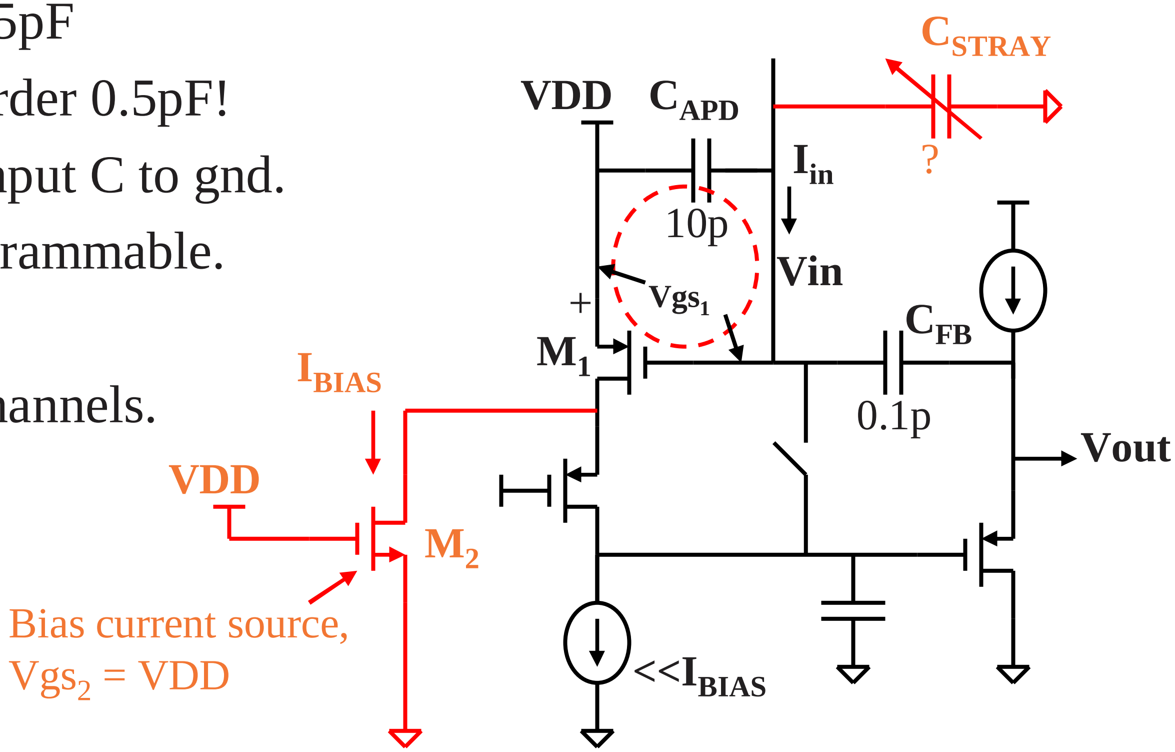
    If (C_{STRAY}/C_{APD}) = (gm_2/gm_1), then **△Vout = 0!!** (to 1st order).

- Typically (gm_2/gm_1) ~ 0.05:

  M2 noise contribution ~ 2%

  Optimum C_{STRAY} ~ 0.5pF

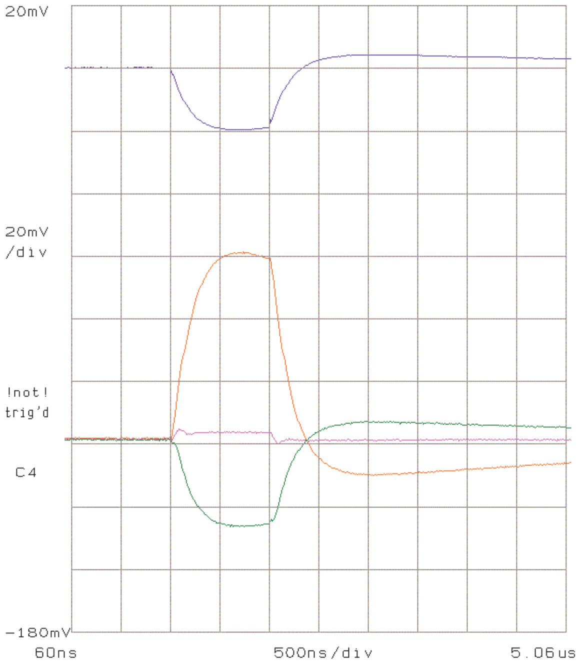
- Unavoidable C_{STRAY} is of order 0.5pF!
- Add small programmable input C to gnd.
- Make I_{BIAS} (M_2 width) programmable.
- Tweak for best PSRR!
- Assumes same C's on all channels.



Bias current source,
Vgs_2 = VDD

Integrator output response to VDD transient

Cin = 15 pF (to VDD) + Cstray (to gnd, programmable)



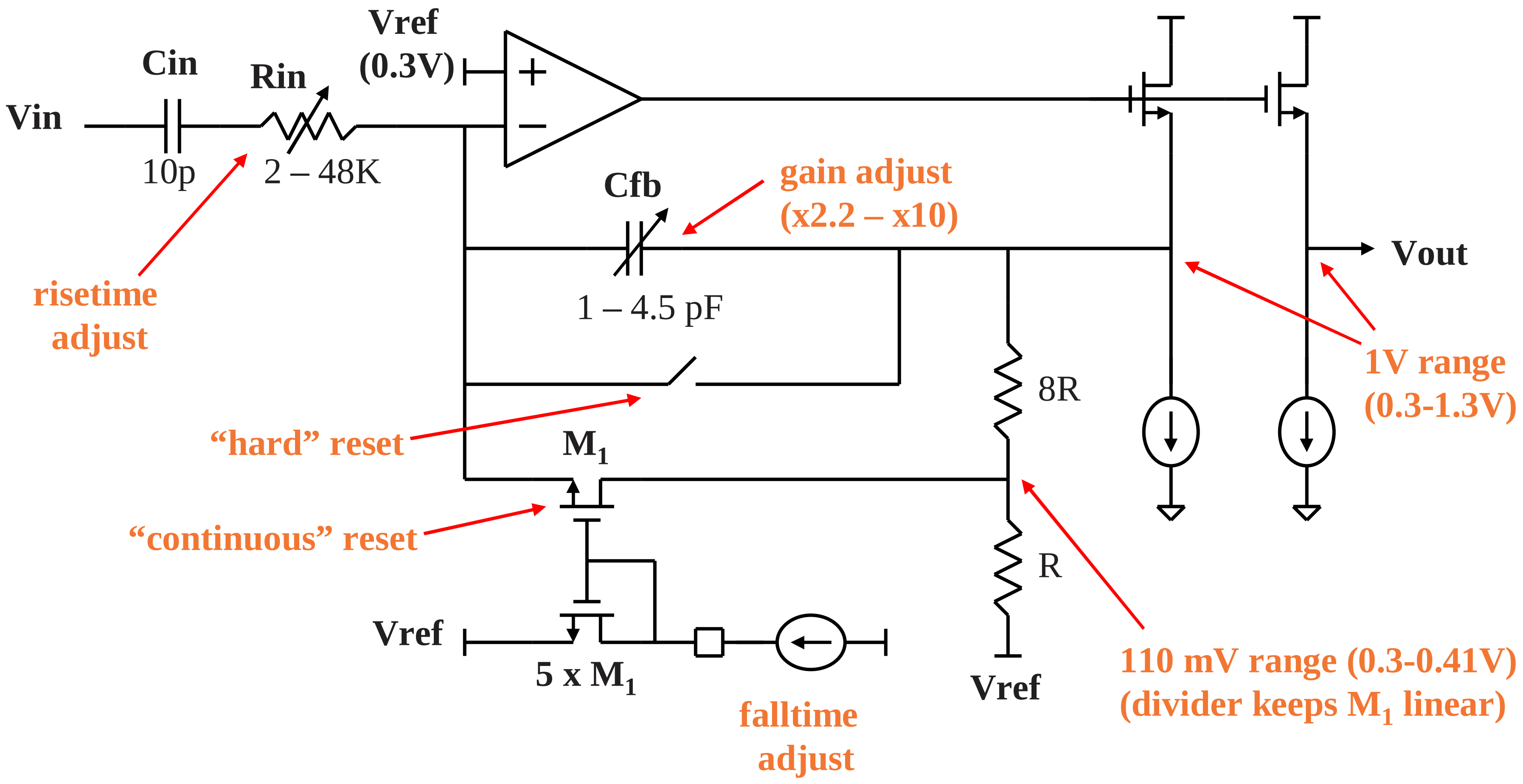
← △VDD = 20 mV (externally forced transient)

← Integrator outputs for 3 different values of Cstray

Tweak Cstray for best VDD immunity!

Shaper

- Risetime set by (RinCin), programmable. Not affected by gain setting.
- Voltage gain set by (Cin/Cfb), programmable. Not affected by risetime setting.
- External adjustment for falltime. Falltime affected by gain setting (Cfb).
- Falltime independent of signal magnitude.



risetime adjust

gain adjust (x2.2 – x10)

1V range (0.3-1.3V)

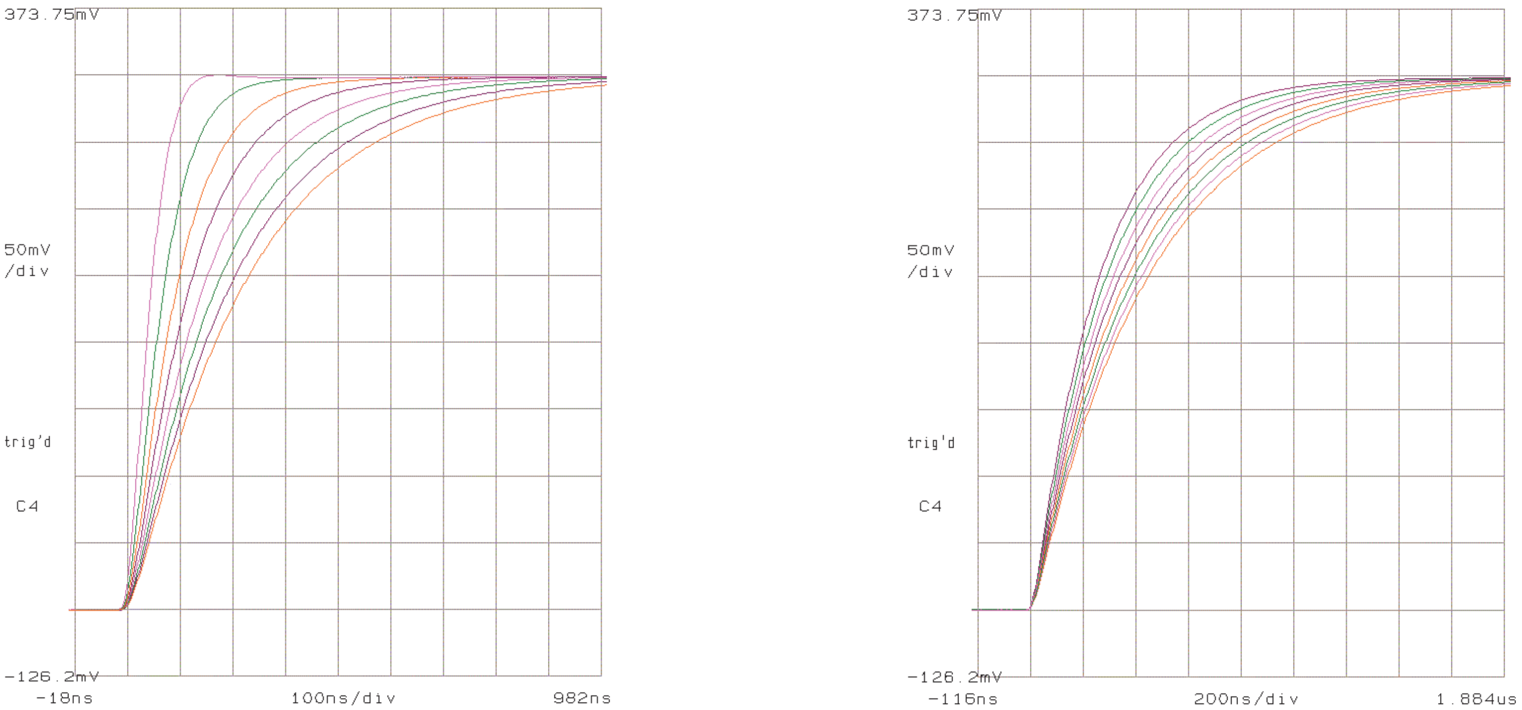
"hard" reset

"continuous" reset

falltime adjust

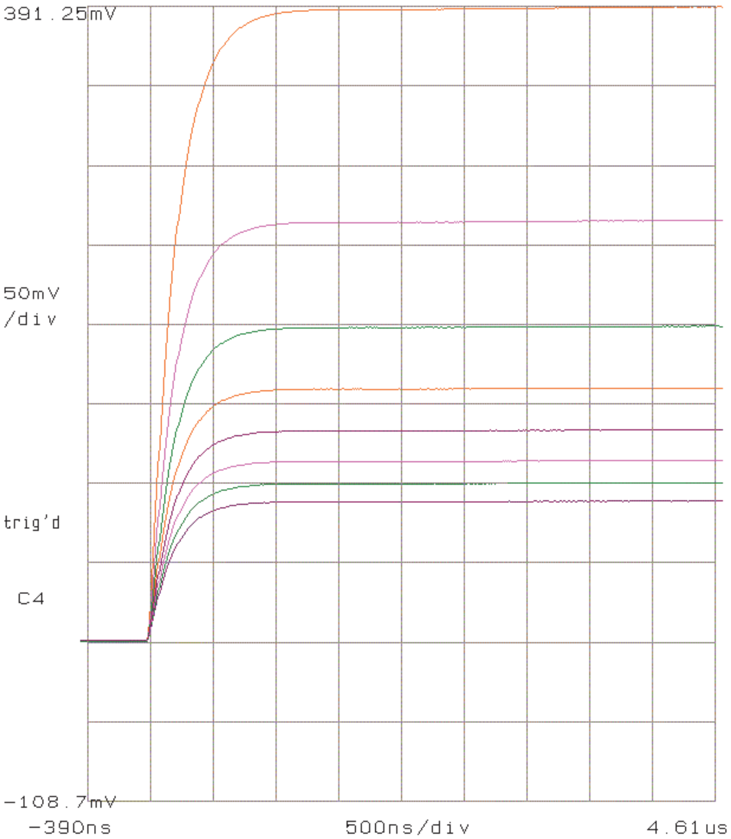
110 mV range (0.3-0.41V) (divider keeps M_1 linear)

Shaper output programmable risetime



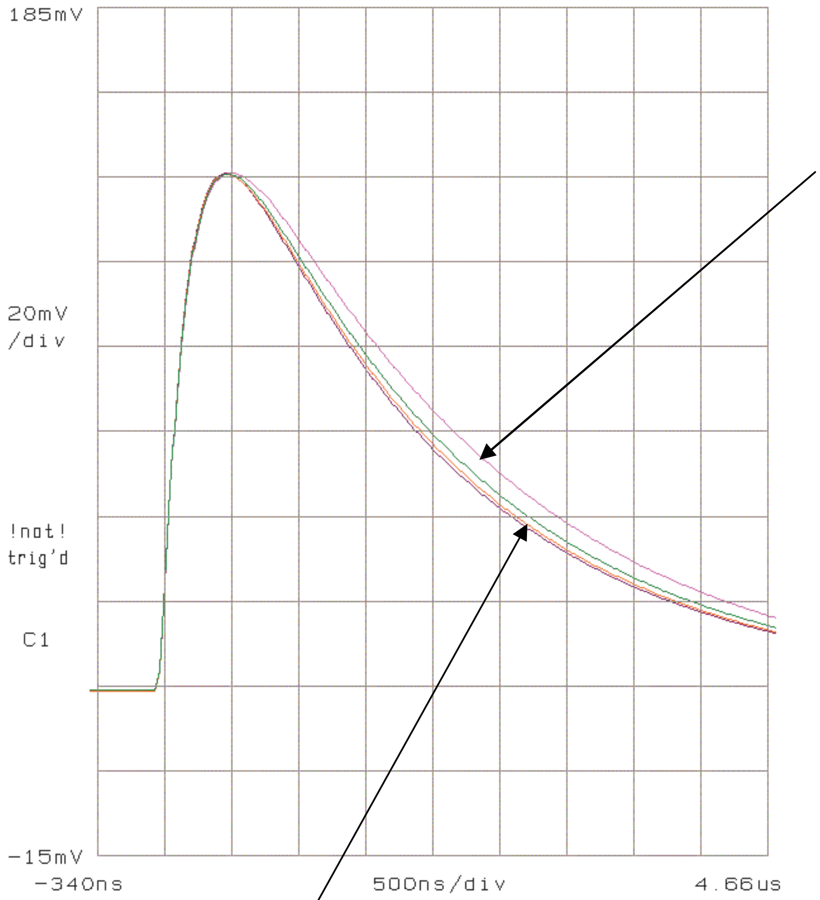
16 settings give risetime from 57 ns to 446 ns

Shaper output programmable gain



8 settings give shaper gain from x2.2 to x10.
No significant effect on risetime.

Shaper output with finite fall time



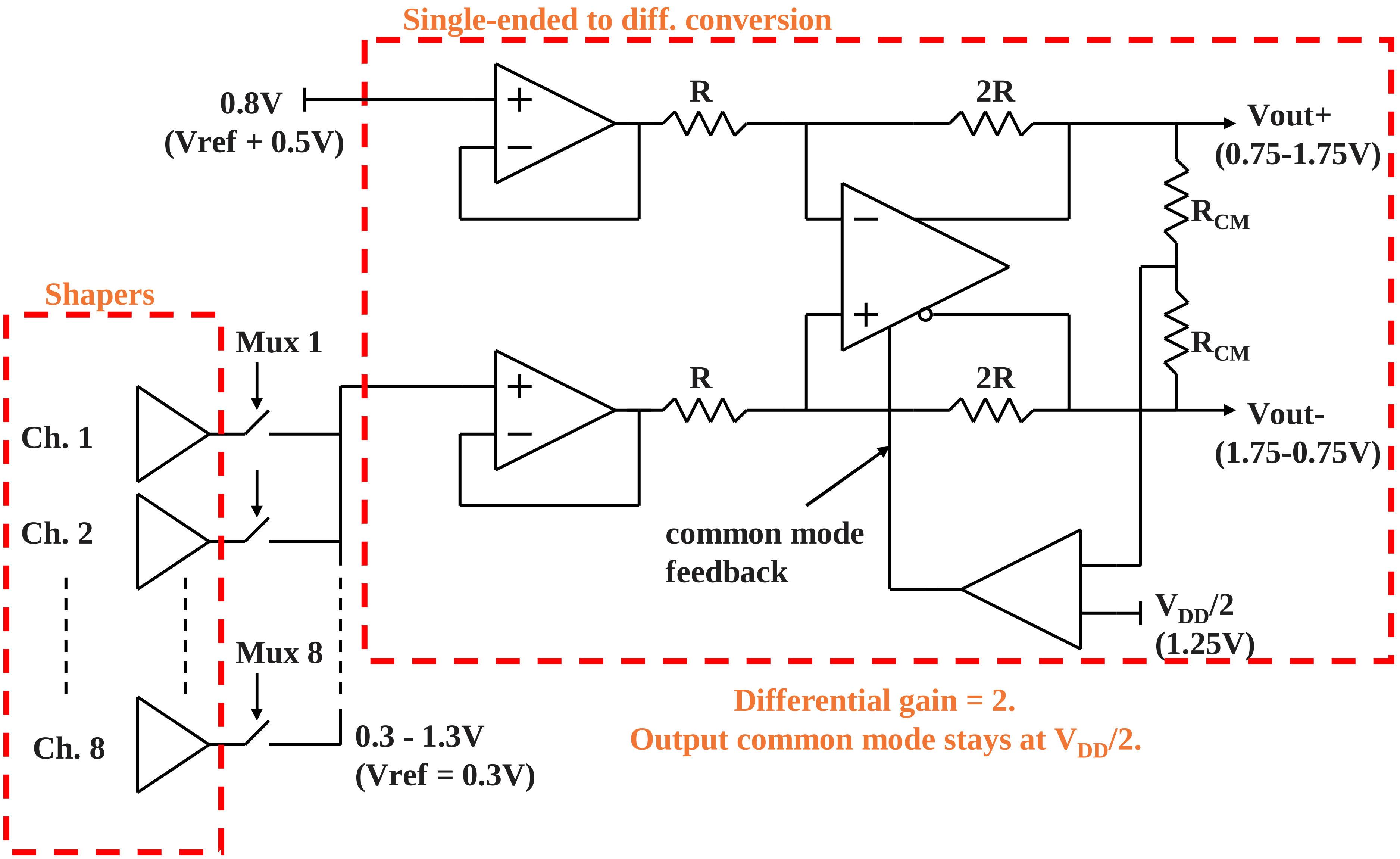
△Vout = 1200 mV

4 values of △Vout:
120, 300, 600, 1200 mV
(normalized)

△Vout = 120 mV

(feedback divider gives relatively stable falltime for different output amplitudes)

Mux Version: single-ended shaper output converted to differential output to drive ADC

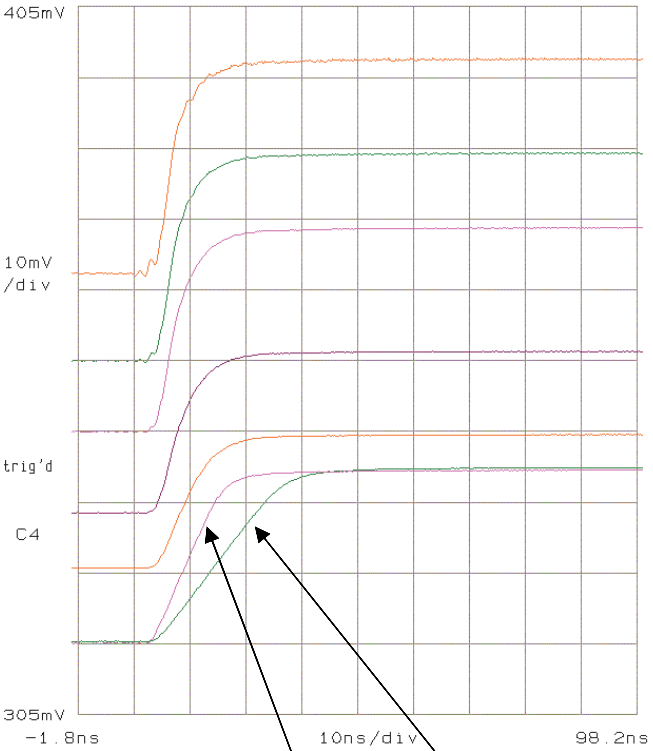


Differential gain = 2.

Output common mode stays at $V_{DD}/2$.

S.E. to diff. amplifier response for different amplitudes (scaled)

Vout+ (positive amplifier output)



△Vout =

30 mV

60 mV

120 mV

240 mV

400 mV

1000 mV

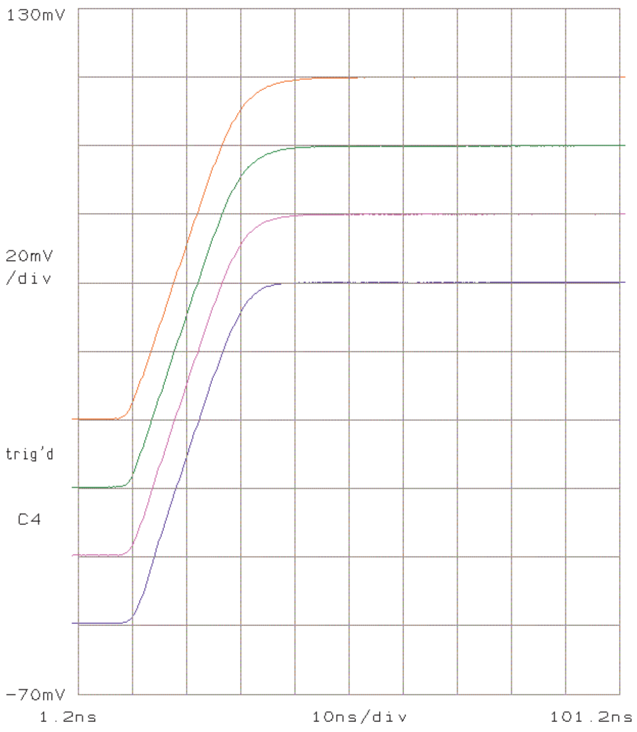
10 ns/div

nominal amp bias

Completely settled in < 40 ns

2X nominal amp bias

Differential output [(Vout+) – (Vout-)] for max. amplitude (2V)



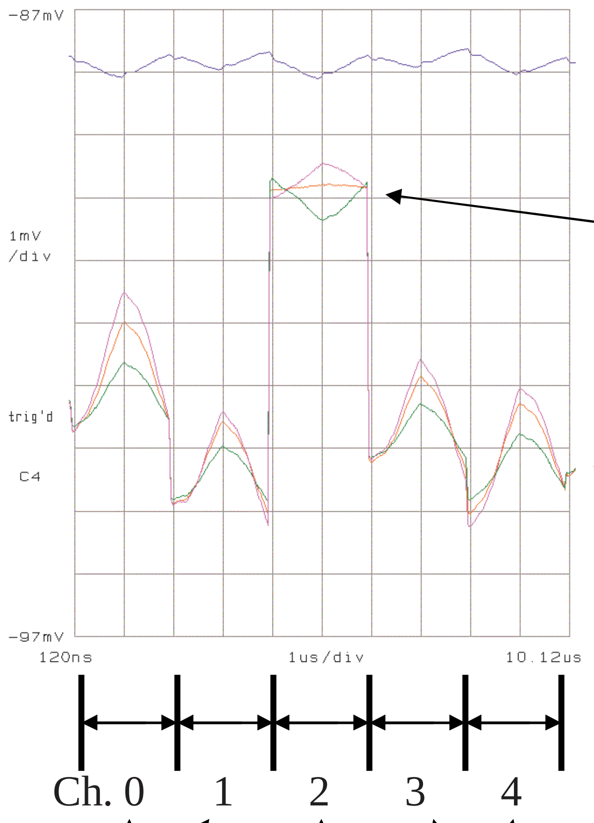
Cout =
0 pF
10 pF
20 pF
30 pF

400
mV/div

10 ns/div

Multiplexer readout with VDD transient

Variations at integrator outputs (amplified by shaper) appear at mux output.



△VDD = 0.3 mV (from operating the mux).
(1 mV/div)

Tweak Cstray for best integrator immunity!
Optimum Cstray depends on Cin to VDD.

Mux readout for 3 different programmed values of Cstray.
(10 mV/div)

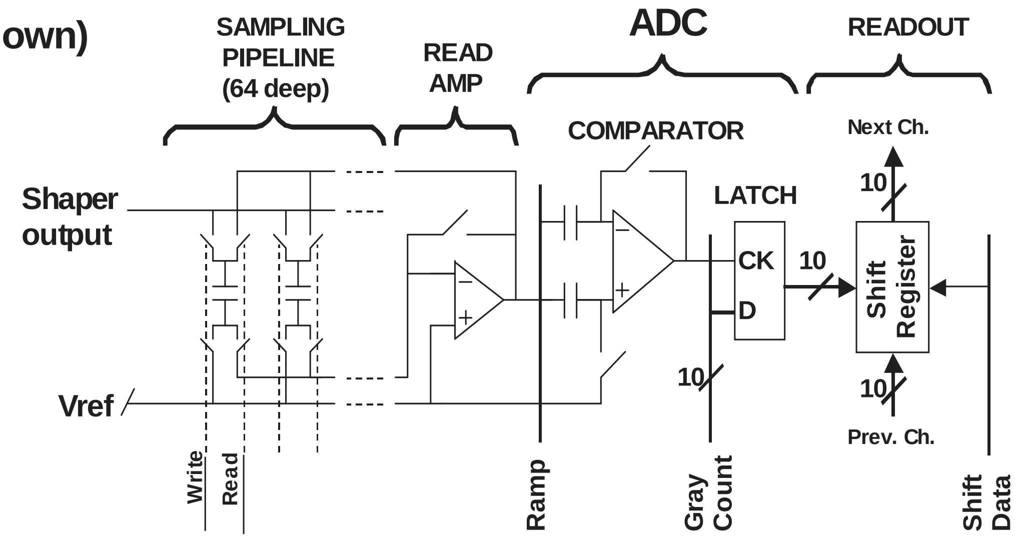
unbonded channels

unbonded channels

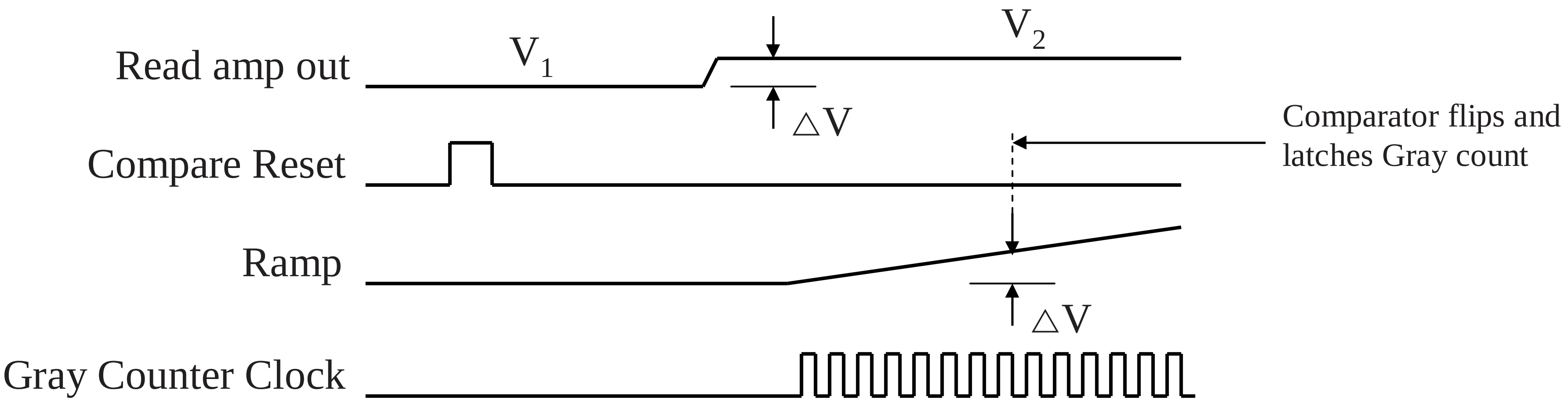
bonded channel,
Cin = 15 pF to VDD

Pipeline Version: 64 deep pipeline + on-chip multichannel Wilkinson ADC

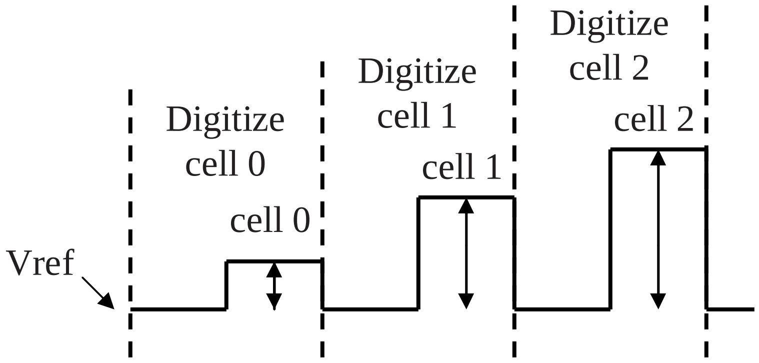
(1 channel shown)



Digitize $\triangle V = (V_2 - V_1)$:



Two digitize options

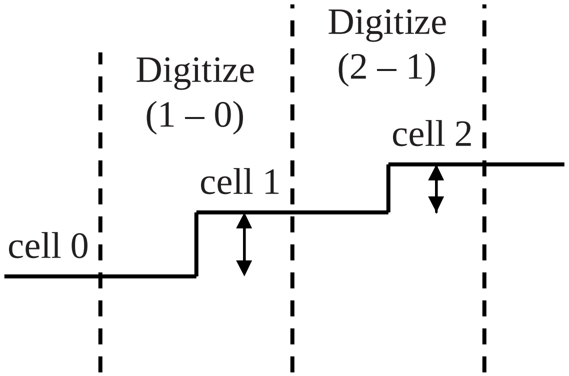


- **Option 1: cell only**

  V1 = Read amp reset voltage (Vref) always

  V2 = Pipeline cell voltage (Vref + excursion due to shaper output)

  The ADC directly digitizes the shaper signal level sampled by each cell of the pipeline. The signal is always positive with respect to Vref.



- **Option 2: DCS**

  V1 = Pipeline cell (n-1) voltage

  V2 = Pipeline cell (n) voltage

The ADC digitizes the difference between two neighboring pipeline cell voltages (dual correlated sampling). Continuous shaper reset should not be used , since only positive differences can be digitized.

Two acquire/digitize modes

- **Mode 1: Separate acquisition and digitization:**

  First acquire signals by filling the pipeline, then stop acquisition.

  Digitize and readout all pipeline cells.

- **Mode 2: Concurrent acquisition and digitization:**

  Acquisition and digitization occur simultaneously (with latency). Range or resolution must be sacrificed in order to digitize every 500 ns.

Progress to date

- The chip is completely functional.
- MUX version: performance is adequate and meets all specs.
- PIPELINE version: only the “Separate acquisition and digitization” mode has been tested. The on-chip ADC digitizes dual correlated samples as desired.
- The DCS digitize option was used to measure noise.
- “Concurrent acquisition and digitization” mode not yet studied. Coupling from digital back end to analog front end???

Noise Measurements

Conditions:

- Integrator input transistor bias current = 1mA
- Shaper rise time constant = 206 ns (hard reset, infinite fall time)
- Shaper gain = X10 (integrator + shaper = 100 mV/fC)
- Dual correlated sample (t = 1000 ns)
- Noise downstream from integrator (shaper + ADC) = 41 electrons (for shaper gain = 10). Subtract this noise from the measurement to get only the integrator noise contribution.
- Many different variations of input transistor W/L.

Integrator Noise Measurements

W/L	DCS noise (e)
880/.32	6e + 8.5e/pF
1200/.32	9e + 7.7e/pF
1540/.32	14e + 7.3e/pF
620/.4	7e + 9.4e/pF
880/.4	5e + 8.4e/pF
1540/.4	19e + 7.5e/pF
620/.6	8e + 9.5e/pF
1540/.6	21e + 7.9e/pF
620/1	23e + 10.2e/pF
1540/1	49e + 8.4e/pF

- Noise slope measurement is accurate
- Noise intercept not as accurate (stray wiring C ~ 7pF subtracted out)

Best: 10 pF noise = 87e
20 pF noise = 160e

- The measured noise is ***lower*** than the simulated noise! High confidence in measurements.
- SVX3 chip noise measurements with NMOS input transistor (TSMC 0.25 u) showed “excess” noise at shorter channel lengths (used L = 0.8u). PMOS shows no such behavior – shorter is better (should have tried L = 0.25u!).